In the Claims:

Please cancel claim 7. Please amend claims 1 and 10. Please add new claim 34. The claims are as follows:

1. (Currently amended) A capacitor formed on a substrate, comprising:

a Fin structure having a top surface and a first side surface opposite a second side surface, said Fin structure including a single-crystal semiconductor material;

an insulator structure adjacent the top surface of the Fin structure; and

a conductor structure adjacent the insulator structure, wherein all conducting material on a top surface of the insulator structure is continuously distributed on the top surface of the insulator structure and is comprised by the conductor structure, wherein the conductor structure partially but not totally overlays the Fin structure, and wherein a thickness of the conductor structure is within a thickness of the Fin structure, said thickness of the Fin structure being a distance between the first and second side surfaces of the Fin structure, said thickness of the conductor structure being oriented in a same direction as said thickness of the Fin structure, said insulator structure comprising a single insulative material distributed from the top surface of the Fin structure to a bottom surface of the conductor structure~~, wherein the thickness of the Fin structure is greater than 40 nm~~.

2. (Previously presented) The capacitor of claim 1, further comprising a first interconnect disposed adjacent to one of the top surface, the first side surface, and the second side surface of the Fin structure.

3. (Previously presented) The capacitor of claim 2, further comprising a second interconnect connected to the conductor structure.

4. (Previously presented) The capacitor of claim 1, wherein the conductor structure includes a conductive material selected from the group consisting of a metal, a metal silicide, and doped polysilicon.

5. (Canceled)

6. (Previously presented) The capacitor of claim 1, wherein the Fin structure has a height between 10 nm and 160 nm.

7. (Canceled)

8. (Original) The capacitor of claim 1, wherein a FinFET is disposed on the substrate, the FinFET having a gate electrode coupled to said conductor structure.

9. (Canceled)

10. (Currently amended) An integrated circuit chip, comprising a first nominal-voltage decoupling capacitor and a second high-voltage decoupling capacitor, respectively comprising:

a first Fin structure having a first thickness and a second ~~single-crystal~~ Fin structure having a second thickness greater than said first thickness, said first Fin structure and said second Fin structure each having a top surface and a first side surface opposite a second side surface, said first thickness being a distance between the first and second side surfaces of the first Fin structure, said second thickness being a distance between the first and second side surfaces of the second Fin structure, said first Fin structure including a single-crystal semiconductor material, said second Fin structure including the single-crystal semiconductor material;

a first insulator structure adjacent the top surface, the first side surface, and the second side surface of the first Fin structure, thereby encapsulating the first Fin structure, and a second insulator structure adjacent the top surface of the second Fin structure; and

a first conductor structure adjacent the first insulator structure, and a second conductor structure adjacent the second insulator structure, wherein the second conductor structure partially but not totally overlays the second Fin structure and a thickness of the second conductor structure is within a thickness of the second Fin structure, and wherein the first conductor structure totally overlays the first Fin structure and a thickness of the first Fin structure is within a thickness of the first conductor structure, said thickness of the first conductor structure being oriented in a same direction as said thickness of the first Fin structure, said thickness of the second conductor structure being oriented in a same direction as said thickness of the second Fin structure, said first insulator structure comprising a single insulative material distributed from the top surface of the first Fin structure to a bottom surface of the first conductor structure, said second insulator structure comprising a single insulative material distributed from the top surface of the second Fin structure to a bottom surface of the second conductor structure.

11. (Previously prescnted) Thc integrated circuit chip of claim 10, wherein said second Fin structure has conductivity-enhancing dopant ions therein.

12-19. (Canceled)

20. (Previously presented) A capacitor formed on a substratc, comprising:

a Fin structure having a top surface and a first side surfacc opposite a second side surface, said Fin structure including a single-crystal semiconductor material;

an insulator structure adjacent the top surfacc of the Fin structure;

a conductor structure adjacent the insulator structure, wherein the conductor structure totally overlays thc Fin structure, wherein a thickness of the Fin structure is within a thickness of the conductor structure, said thickness of the Fin structure being a distance between the first and second side surfaces of thc Fin structure, said thickness of the conductor structure being oriented in a same direction as said thickness of the Fin structure, said insulator structure comprising a single insulative material distributed from the top surface of the Fin structure to a bottom surface of the conductor structure; and

an insulator layer such that an entire bottom surface of thc Fin structure is in direct mechanical contact with a top surfacc of the insulator layer.

21. (Previously presented) The capacitor of claim 20, further comprising a first interconnect disposed adjacent to one of thc top surface, thc first side surface, and the second side surfacc of

the Fin structure.

22. (Previously presented) The capacitor of claim 21, further comprising a second interconnect connected to the conductor structure.

23. (Canceled)

24. (Previously presented) The capacitor of claim 20, wherein the thickness of the Fin structure is in a range of 0.3 nm to 40 nm.

25. (Previously presented) The capacitor of claim 20, wherein the Fin structure has a height between 10 nm and 160 nm.

26. (Canceled)

27. (Previously presented) The capacitor of claim 20, wherein a FinFET is disposed on the substrate, the FinFET having a gate electrode coupled to said conductor structure.

28. (Canceled)

29. (Previously presented) The capacitor of claim 20, wherein a thickness of the insulator structure is about equal to the thickness of the Fin structure, said thickness of the insulator

structure being oriented in a same direction as said thickness of the Fin structure.

30. (Previously presented) The capacitor of claim 20, further comprising an insulation film on the first side surface of the Fin structure and in direct mechanical contact with the first side surface of the Fin structure, wherein the insulator structure has a lower surface and an upper surface such that a height of the lower surface of the insulator structure above the top surface of the insulator layer is less than a height of the upper surface of the insulator structure above the top surface of the insulator layer, and wherein a height of a top surface of the insulation film above the top surface of the insulator layer is greater than the height of the lower surface of insulator structure and less the height of the upper surface of the insulator structure.

31. (Previously presented) The capacitor of claim 30, wherein the insulation film includes an insulator material that differs from the single insulative material.

32. (Previously presented) The capacitor of claim 1, further comprising:

an insulator layer such that an entire bottom surface of the Fin structure is in direct mechanical contact with a top surface of the insulator layer; and

an insulation film on the first side surface of the Fin structure and in direct mechanical contact with the first side surface of the Fin structure, wherein the insulator structure has a lower surface and an upper surface such that a height of the lower surface of the insulator structure above the top surface of the insulator layer is less than a height of the upper surface of the insulator structure above the top surface of the insulator layer, and wherein a height of a top

surface of the insulation film above the top surface of the insulator layer is greater than the height of the lower surface of insulator structure and less the height of the upper surface of the insulator structure.

33. (Previously presented) The capacitor of claim 32, wherein the insulation film includes an insulator material that differs from the single insulative material.

34. (New) The capacitor of claim 1, wherein the thickness of the Fin structure is greater than 40 nm.